PALM INTRANET

Day : Thursday
Date: 11/16/2006
Time: 13:40:18

Inventor Name Search Result

Your Search was:

Last Name = MOON
First Name = YONGSAM

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08920336	5955929	150	08/27/1997	VOLTAGE-CONTROLLED OSCILLATOR RESISTANT TO SUPPLY VOLTAGE NOISE	MOON, YONGSAM
09007707	5969552	150	01/15/1998	DUAL LOOP DELAY-LOCKED LOOP	MOON, YONGSAM
09234777	6600771	150	01/20/1999	SPREAD SPECTRUM PHASE MODULATION FOR SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS	MOON, YONGSAM
09948123	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	MOON, YONGSAM
10305254	Not Issued	161	11/25/2002	0.6-2.5 GBaud CMOS tracked 3X oversampling transceiver with dead zone phase detection for robust clock/data recovery	MOON, YONGSAM
10356695	6859107	150	01/30/2003	FREQUENCY COMPARATOR WITH HYSTERESIS BETWEEN LOCKED AND UNLOCKED CONDITIONS	MOON, YONGSAM
10612840	Not Issued	30	07/03/2003	Tracked 3X oversampling receiver	MOON, YONGSAM
10613442	6888417	150	07/03/2003	VOLTAGE CONTROLLED OSCILLATOR	MOON, YONGSAM
10651500	Not Issued	41	08/29/2003	CMOS transceiver with dual current path VCO	MOON, YONGSAM
10652721	Not Issued	160	08/29/2003	CMOS transceiver with dual current path VCO	MOON, YONGSAM
10722842	6876240	150	11/25/2003	WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP	MOON, YONGSAM
60026106	Not Issued	159	08/27/1996	SUPPLY NOISE INDEPENDENT VOLTAGE CONTROLLED OSCILLATOR	MOON, YONGSAM
60071805	Not Issued	159	01/20/1998	SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS THROUGH SPREAD SPECTRUM PHASE MODULATION	MOON, YONGSAM
60230589	Not Issued	159	09/05/2000	Oversampling transceiver with dead-zone phase detection	MOON, YONGSAM
60333439	Not Issued	159	11/26/2001	0.6-2.5GBaud CMOS tracked 3x oversampling transceiver with dead-zone phase detection for robust clock/data recovery	MOON, YONGSAM
60406858	Not Issued	159	08/29/2002	CMOS transceiver with dual current path VCO	MOON, YONGSAM
60590710	Not Issued	159	07/22/2004	Divide-by-16.5 frequency divider with cascaded divide-by-3 and divide-by-5.5 dividers and devices including same	MOON, YONGSAM

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = AHN
First Name = GIJUNG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09146818	6229859	150	09/04/1998	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	AHN, GIJUNG
09234619	6560290	150	01/20/1999	CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABAUD SPEED DATA COMMUNICATION	AHN, GIJUNG
09814256	6587525	150	03/21/2001	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	AHN, GIJUNG
09948123	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	AHN, GIJUNG
10171860	7088398	150	06/14/2002	METHOD AND APPARATUS FOR REGENERATING A CLOCK FOR AUXILIARY DATA TRANSMITTED OVER A SERIAL LINK WITH VIDEO DATA	AHN, GIJUNG
10192296	6914637	150	07/10/2002	METHOD AND SYSTEM FOR VIDEO AND AUXILIARY DATA TRANSMISSION OVER A SERIAL LINK	AHN, GIJUNG
10305254	Not Issued	161	11/25/2002	0.6-2.5 GBaud CMOS tracked 3X oversampling transceiver with dead zone phase detection for robust clock/data recovery	AHN, GIJUNG
10356695	6859107	150	01/30/2003	FREQUENCY COMPARATOR WITH HYSTERESIS BETWEEN LOCKED AND UNLOCKED CONDITIONS	AHN, GIJUNG
10612840	Not Issued	30	07/03/2003	Tracked 3X oversampling receiver	AHN, GIJUNG
10613442	6888417	150	07/03/2003	VOLTAGE CONTROLLED OSCILLATOR	AHN, GIJUNG
10658590	Not Issued	30	09/08/2003	Method and apparatus for double data rate serial ATA phy interface	AHN, GIJUNG
10722842	6876240	150	11/25/2003	WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP	AHN, GIJUNG
10781405	Not Issued	71	02/18/2004	Cable with circuitry for asserting stored cable data or other information to an external device or user	AHN, GIJUNG
60058040	Not Issued	159	09/04/1997	DATA RECOVERY SCHEME FOR OVERSAMPLED SYSTEMS	AHN, GIJUNG
60071879	Not Issued	159	01/20/1998	1.25GBAUD CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABIT ETHERNET PHY CHIP	AHN, GIJUNG
60230589	Not Issued	159	09/05/2000	Oversampling transceiver with dead-zone phase detection	AHN, GIJUNG
60333439	Not Issued	159	11/26/2001	0.6-2.5GBaud CMOS tracked 3x oversampling transceiver with dead-zone phase detection for robust clock/data recovery	AHN, GIJUNG
60406858	Not Issued	159	08/29/2002	CMOS transceiver with dual current path VCO	AHN, GIJUNG
60760601	Not Issued	20	01/20/2006	Concurrent code checker: hardware efficient HSIO built-in self-test & debug structure	AHN, GIJUNG

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = JEONG
First Name = DEOG-KYOON

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08000430	5332934	150	01/04/1993	SMALL TO FULL SWING CONVERSION CIRCUIT	JEONG, DEOG-KYOON
08254326	5714904	150	06/06/1994	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
08332561	5574756	150	10/31/1994	METHOD FOR GENERATING DIGITAL COMMUNICATION SYSTEM CLOCK SIGNALS & CIRCUITRY FOR PERFORMING THAT METHOD	JEONG, DEOG-KYOON
08370904	5621407	150	01/10/1995	DIGITAL/ANALOG CONVERTER	JEONG, DEOG-KYOON
08415056	5712884	150	03/31/1995	DATA RECEIVING METHOD AND CIRCUIT OF DIGITAL COMMUNICATION SYSTEM	JEONG, DEOG-KYOON
08580569	5705947	150	12/29/1995	CLOCK GENERATOR	JEONG, DEOG-KYOON
08580571	5587709	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
08580700	5675584	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
08580914	5712585	150	12/29/1995	A SYSTEM FOR DISTRIBRITING CLOCK SIGNALS	JEONG, DEOG-KYOON
08581135	5802103	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
08631420	5815041	150	04/12/1996	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	JEONG, DEOG-KYOON
08664136	5835498	150	06/14/1996	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK	JEONG, DEOG-KYOON
08815486	6157360	150	03/11/1997	SYSTEM AND METHOD FOR DRIVING COLUMNS OF AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
08920336	5955929	150	08/27/1997	VOLTAGE-CONTROLLED OSCILLATOR RESISTANT TO SUPPLY VOLTAGE NOISE	JEONG, DEOG-KYOON
08937262	6100868	150	09/15/1997	HIGH DENSITY COLUMN DRIVERS FOR AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
09007707	5969552	150	01/15/1998	DUAL LOOP DELAY-LOCKED LOOP	JEONG, DEOG-KYOON
09013679	6211714	150	01/26/1998	PARALLEL CONDUCTOR SYSTEM FOR REDUCING NOISE IN TRANSMITTING CLOCK SIGNALS	JEONG, DEOG-KYOON
09017758	6107946	150	02/03/1998	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
09098266	6157263	150	06/16/1998	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	JEONG, DEOG-KYOON
09146818	6229859	150	09/04/1998	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	JEONG, DEOG-KYOON
09148583	6271816	150	09/04/1998	POWER SAVING CIRCUIT AND METHOD FOR DRIVING AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
09148815	6144242	150	09/04/1998	CONTROLLABLE DELAYS IN MULTIPLE SYNCHRONIZED SIGNALS FOR REDUCED ELECTROMAGNETIC INTERFERENCE AT PEAK FREQUENCIES	JEONG, DEOG-KYOON
09187559	6151334	150	11/04/1998	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK	JEONG, DEOG-KYOON
09234619	6560290	150	01/20/1999	CMOS DRIVER AND ON-CHIP TERMINATION FOR	JEONG, DEOG-KYOON

				GIGABAUD SPEED DATA COMMUNICATION	
09234777	6600771	150	01/20/1999	SPREAD SPECTRUM PHASE MODULATION FOR SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS	JEONG, DEOG-KYOON
09298369	6374361	150	04/22/1999	SKEW-INSENSITIVE LOW VOLTAGE DIFFERENTIAL RECEIVER	JEONG, DEOG-KYOON
09393849	6738417	150	09/09/1999	METHOD AND APPARATUS FOR BIDIRECTIONAL DATA TRANSFER BETWEEN A DIGITAL DISPLAY AND A COMPUTER	JEONG, DEOG-KYOON
09574571	6326826	150	05/17/2000	Wide frequency-range delay-locked loop circuit	JEONG, DEOG-KYOON
09693516	6462624	150	10/20/2000	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP	JEONG, DEOG-KYOON
09709637	6483355	150	11/13/2000	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	JEONG, DEOG-KYOON
09759624	6891910	150	01/12/2001	BAUD-RATE TIMING RECOVERY	JEONG, DEOG-KYOON
09766503	Not Issued	160	01/18/2001	High speed serial link for fully duplexed data communication	JEONG, DEOG-KYOON
09814256	6587525	150	03/21/2001	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	JEONG, DEOG-KYOON
09897975	6510185	150	07/05/2001	SINGLE CHIP CMOS TRANSMITTER/RECEIVER	JEONG, DEOG-KYOON
09943029	Not Issued	161	08/29/2001	Data recovery using data eye tracking	JEONG, DEOG-KYOON
09948123	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	JEONG, DEOG-KYOON
09985897	6512408	150	11/06/2001	MIXER STRUCTURE AND METHOD FOR USING SAME	JEONG, DEOG-KYOON
10035591	Not Issued	41	11/07/2001	Communications architecture for storage-based devices	JEONG, DEOG-KYOON
10035911	Not Issued	95	11/07/2001	METHOD AND SYSTEM FOR NESTING OF COMMUNICATIONS PACKETS	JEONG, DEOG-KYOON
10036135	Not Issued	61	11/07/2001	Method and system for packet ordering based on packet type	JEONG, DEOG-KYOON
10036794	6976201	150	11/07/2001	METHOD AND SYSTEM FOR HOST HANDLING OF COMMUNICATIONS ERRORS	JEONG, DEOG-KYOON
10037168	Not Issued	61	11/07/2001	Method and system for plesiosynchronous communications with null insertion and removal	JEONG, DEOG-KYOON
10045297	Not Issued	71	11/07/2001	Communications architecture for memory-based devices	JEONG, DEOG-KYOON
10045348	Not Issued	41	11/07/2001	Method and system for asymmetric packet ordering between communications devices	JEONG, DEOG-KYOON
10045393	7039121	150	11/07/2001	METHOD AND SYSTEM FOR TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION COMMUNICATIONS	JEONG, DEOG-KYOON
10045600	6771192	150	11/07/2001	METHOD AND SYSTEM FOR DC-BALANCING AT THE PHYSICAL LAYER	JEONG, DEOG-KYOON
10045601	Not Issued	121	11/07/2001	Multisection memory bank system	JEONG, DEOG-KYOON
10045606	Not Issued	161	11/07/2001	Method and system for dynamic segmentation of communications packets	JEONG, DEOG-KYOON
10045625	Not Issued	41	11/07/2001	Method and system for integrating packet type information with synchronization symbols	JEONG, DEOG-KYOON
10053461	7113507	150	11/07/2001	METHOD AND SYSTEM FOR COMMUNICATING CONTROL INFORMATION VIA OUT-OF-BAND SYMBOLS	JEONG, DEOG-KYOON

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